PATENT

43269

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	
	:	
Stephen Liscinsky	:	Appeal No. _____
	:	
Serial No.: 10/085,138	:	Patent Art Unit: 2836
	:	
Filed: March 1, 2002	:	Examiner: Kito, Zeev
	:	
For: A THREE PHASE SUPERVISORY CIRCUIT	:	

APPELLANT'S BRIEF ON APPEAL UNDER 37 C.F.R. § 1.192

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

For the appeal to the Board of Patent Appeals and Interferences from the decision dated August 5, 2003 of the primary Examiner finally rejecting claims 1-18 in connection with the above-identified application, Appellant submits the following brief (in triplicate) in accordance with 37 C.F.R. § 1.192.

TABLE OF CONTENTS

I. Real Party in Interest

The real party in interest in this application is assignee Hubbell Incorporated. This application was assigned to Hubbell Incorporated by the inventor in an assignment recorded on May 22, 2002 at Reel 012925, Frame 0824.

II. Related Appeals and Interferences

There are no other related appeals or interferences known to Appellant, Appellant's legal representative, or Assignee, which would directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of the Claims

Claims 1-18 are pending, and claims 1-18 are on appeal. No claim is allowed.

In the Final Office Action dated August 8, 2003, claims 1, 4 - 6, 11, 12, 14 - 18 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 3,535,591 to Holmquest (hereinafter Holmquest) in view of U.S. Patent 5,224,010 to Tran et al. (hereinafter Tran).

Additionally, in the final Office Action, claims 8 - 10 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Holmquest in view of Tran and further in view of U.S. Patent 5,642,052 to Earle.

Also, in the final Office Action, claims 2 and 13 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Holmquest in view of Tran and further in view of the Court Decision In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955).

Finally, in the final Office Action, claims 3 and 15 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Holmquest in view of Tran and further in view of the Court Decision In re Bosch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

IV. Status of the Amendments

No amendment was filed subsequent to the final rejection of August 5, 2003.

V. Summary of the Invention

The present invention is a method and apparatus for monitoring a three phase power signal for a change in operating conditions. Specifically, the present invention is a three phase supervisory circuit for detecting fault conditions in an input AC power signal. The three phase supervisory circuit includes a first sensing circuit for detecting a voltage level for a first phase of said AC power signal and comparing the voltage level of the first phase to a threshold value. A second sensing circuit for detecting a voltage level for a second phase of the AC power signal and comparing the voltage level of the second phase to the threshold value. The three phase supervisory circuit further includes a third sensing circuit for detecting a voltage level for a third phase of the AC power signal and comparing the voltage level of the third phase to the threshold value. A delay circuit for delaying initial operation of the sensing circuits for a predetermined period each time the supervisory circuit is powered on, and an activation circuit for receiving indication signals from the sensing and delay circuits, the indication signals indicative of whether

the predetermined period of time has elapsed and the voltage levels of the phases have met the threshold value.

The three phase supervisory circuit is able to detect a fault resulting in a change in operating conditions. The fault can include an open neutral in any one of an AC line input, an open first phase, an open second phase, an open third phase, reverse wiring of the first phase to the neutral, reverse wiring of the second phase to the neutral, reverse wiring of the third phase to the neutral, and duplicative wiring of any of the phases. In this manner, proper wiring and proper phase relationships can be verified for each wire and phase.

VI. Issue for Review

The following issues are presented for review.

1. Whether claims 1, 4 - 6, 11, 12, 14 - 18 are obvious and unpatentable under 35 U.S.C. § 103(a) over U.S. Patent 3,535,591 to Holmquest in view of U.S. Patent 5,224,010 to Tran.

2. Whether claims 8 - 10 are obvious and unpatentable under 35 U.S.C. § 103(a) over Holmquest in view of Tran and further in view of U.S. Patent 5,642,052 to Earle.

3. Whether claims 2 and 13 are obvious and unpatentable under 35 U.S.C. § 103(a) over Holmquest in view of Tran and further in view of the Court Decision In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955).

4. Whether claims 3 and 15 are obvious and unpatentable under 35 U.S.C. § 103(a) as being unpatentable over Holmquest in view of Tran and further in view of the Court Decision In re Bosch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

VII. Grouping of the Claims

For purposes of this appeal, independent claims 1 and 12 and corresponding dependent claims 2-11, and 13-16 stand or fall together. Independent claims 17 and 18 stand or fall together for the reasons discussed herein.

VIII. Argument

In the November 25, 2003 Advisory Action, claims 1, 4 - 6, 11, 12, 14 - 18 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 3,535,591 to Holmquest in view of U.S. Patent 5,224,010 to Tran et al. Claims 8 - 10 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Holmquest in view of Tran and further in view of U.S. Patent 5,642,052 to Earle. Claims 2 and 13 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Holmquest in view of Tran and further in view of the Court Decision In re Aller, 105 USPQ 233. Claims 3 and 15 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Holmquest in view of Tran and further in view of the Court Decision In re Bosch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Appellant submits that none of the prior art discloses delaying initial operation of sensing circuits or detecting fault conditions from a group consisting of an open neutral in any one of the AC line inputs, an open first phase, an open second phase, an open third phase, reverse wiring of the first phase to the neutral, reverse wiring of the second phase to the neutral, reverse wiring of the third phase to the neutral, and duplicative wiring of any of the phases.

The Examiner admits that the Holmquest does not clearly state when the delay occurs. However, the Examiner relies on the combination of the Holmquest patent with the Tran patent

to show that, in view of the cited art, it would have been obvious to delay the operation of the sensing circuits each time the supervisory circuit is powered on.

The Examiner suggests that although the circuit disclosed in the Tran patent has nothing to do with the AC or DC supervision, "the delay circuit is built in the part of the device, which is remote from the primary voltage sensors (dealing with DC voltage supervision) by at least a couple of stages. At this location, the delay circuit structure and activity is not affected at all by a character of monitored voltage (whether it is AC or DC)."

However, the supervision circuit in the Tran patent also includes sensing circuits. The operation of the sensing circuits are not delayed each time the supervisory circuit is powered on. Since, the Tran patent does not disclose delaying its own sensing circuits, it cannot be used in combination with the Holmquest patent to show that the sensing circuits disclosed in the Holmquest patent can be delayed.

For the reasons discussed below, the claimed invention is not obvious over the combination of references cited by the Examiner.

A. <u>None of the cited references teach a delay circuit for delaying initial operation of sensing circuits for a predetermined period each time the supervisory circuit is powered on.</u>

Appellant respectfully disagree that the Holmquest patent discloses, teaches or suggests a delay circuit for delaying initial operation of sensing circuits for a predetermined period each time the supervisory circuit is powered on. Rather, the Holmquest patent, in column 4, lines 32-33 thereof, discloses a time delay in operation of relay 23 which is preset but variable as a function of input parameters. That is, the delay disclosed in the Holmquest patent is based on the sensing circuits detecting the input parameters. Hence, the delay disclosed in the Holmquest

patent can be considered a post-detection delay. In contrast, the independent claims 1 and 12 refer to a delay occurring *prior* to the sensing circuits being operational. Thus, the delay recited in independent claims 1 and 12 is a pre-detection delay in contrast to the time delay based on the sensing circuit disclosed in the Holmquest patent.

In addition, the delay disclosed in the Holmquest patent refers to the delay of opening or closing a relay based on the input parameters. For example, if the difference between an input parameter and a threshold value is small, the response time for closing the relay 23 is slow. However, if there is a large difference between the input parameter and the threshold value, the response time for closing relay 23 is short. This takes "care of momentary variations in voltage, frequency or phase (col. 1, lines 71-72). Thus, the delay disclosed in the Holmquest patent reduces false trips related to minor fluctuations in the input parameter by adjusting the response time for closing the relay 23.

In contrast, the delay in the embodiment of the invention recited in independent claims 1 and 12, does not delay the operation of a relay. Instead, the delay is used to delay the initial operation of the sensing circuits each time the supervisory circuit is powered on. This is quite different from the delay disclosed in the Holmquest patent.

Similarly Appellant disagrees that the Tran patent discloses, teaches or suggest a delay circuit for delaying initial operation of sensing circuits for a predetermined period each time the supervisory circuit is powered on. Specifically, FIG. 2 of the Tran patent discloses a plurality of sensing circuits comprising UV detect 24, OV detect 26, OV scaler 21, and UV scaler 25. The plurality of sensing circuits receive DC input voltages as shown in column 4 lines 19-24, "five inputs in power supply supervisor 15, namely +5IN, +12MIN, +12AIN, _5IN, and –12IN, corresponding to the +5 volt, +12 volt (main and auxiliary), -5 volt, and –12 volt power supply

voltages generated by regulated power supply 13." *After* the input voltages are monitored, either a "PWRGOOD" or a "SHUTDOWN" signal will be issued. Specifically, if an under voltage or over voltage condition is detected, the "PWRGOOD" signal will be delayed (col. 6 lines 31-39). More specifically, the delay is for the DC power supply to stabilize and *not* for the sensing circuits. In fact, the Tran patent does not disclose providing a delay for the sensing circuits, as recited in independent claims 1 and 12 of Appellants' invention.

Thus, the Tran patent does not disclose, teach or suggest a delay circuit for delaying initial operation of sensing circuits for a predetermined period each time the supervisory circuit is powered on as recited in independent claims 1 and 12.

In addition, the Earle patent does not disclose, teach or suggest a delay circuit for delaying initial operation of sensing circuits for a predetermined period each time the supervisory circuit is powered on as recited in independent claims 1 and 12. Instead, the delay disclosed in the Earle patent refers to "a delay circuit 110 that allows the display 108 to be maintained even after the plug 16 has been removed from the receptacle 22" (col. 6, lines 38 – 40). Specifically, the delay disclosed in the Earle patent allows a display to maintain a reading so that a user can still observe the reading after AC power is removed from the device. This is not related to delaying the initial operation of sensing circuits as recited in independent claims 1 and 12.

B. None of the cited references teach sensing circuits being operable to detect fault conditions, the fault conditions being selected from a group consisting of an open neutral in any one of the AC line inputs, an open first phase, an open second phase, an open third phase, reverse wiring of the first phase to the neutral, reverse wiring of the second phase to the neutral, reverse wiring of the third phase to the neutral, and duplicative wiring of any of the phases.

The Holmquest patent does not disclose, teach or suggest sensing circuits being operable to detect fault conditions, the fault conditions being selected from a group consisting of an open neutral in any one of the AC line inputs, an open first phase, an open second phase, an open third phase, reverse wiring of the first phase to the neutral, reverse wiring of the second phase to the neutral, reverse wiring of the third phase to the neutral, and duplicative wiring of any of the phases as recited in independent claims 17 and 18. The system disclosed in the Holmquest patent is limited to the detection of an over or under voltage condition, an over or under frequency condition, and an abnormal phase sequence condition.

The Examiner contends that when more than one phase is open, the system disclosed in the Holmquest patent can detect the condition because an open circuit condition is an extreme case of under voltage condition. However, FIG. 1 of the Holmquest patent discloses a *single* phase sensor. Thus, the system disclosed in the Holmquest patent can only detect one phase condition. The system disclosed in FIG. 1 of Appellant's application shows three sensors for detecting phase and voltage conditions. Thus, specific phase relationships can be detected among the three phases.

Similarly the system disclosed in the Earle patent is a single phase ground fault circuit interrupting (GFCI) device. Therefore, the system disclosed in the Earle patent cannot check for fault conditions in more than one phase. In addition, the Earle patent discloses, "Notably, not all

fault conditions are necessarily tested for. If, for example, the ground and neutral lines 36, 38 are reversed, or if two hot wires have been connected to the receptacle 22, or if a ground path exists, but is of poor quality, the tester 10 may not detect such conditions" (col. 4, lines 54 – 58).

In addition, the system disclosed in the Tran patent is only applicable to DC power systems. As is commonly known to those in the art, DC power has *no phase*. Therefore, the system disclosed in the Tran patent cannot be used for phase detection. Specifically, the system disclosed in the Tran patent checks only for over voltage and under voltage conditions for a DC power supply.

C. <u>One of ordinary skill in the art would not be motivated to combine the references cited by the Examiner</u>

A prima facie obviousness determination requires a showing of the motivation to combine the teachings of the prior art to obtain the claimed method or apparatus. *In re Dembiczak*, 50 USPQ2d 1614 (Fed. Cir. 1999). Obviousness cannot be established by showing that the teachings can be combined, where the motivation to make the combination is lacking. Obviousness requires a showing that one skilled in the art would be lead to make the proposed modification in the manner proposed by the Examiner.

One of skill in the art would not be motivated to combine the Holmquest patent with the Tran patent or the Earle patent. While the Holmquest patent discloses a single phase testing system, the Earle patent also discloses a single phase testing system and the Tran patent discloses a DC power system. Thus, none of the prior art can distinguish between phases. In addition, none of the prior art discloses delaying sensing circuits. The mere fact that the prior art can be modified does not make the modification obvious, unless the art suggests the desirability of the

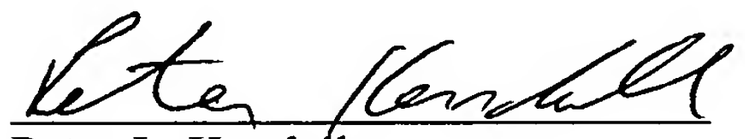
modification. See *In re Laskowski*, 871 F.2d 115, 10 USPQ 2d 1397 (Fed. Cir. 1989). Determination of obviousness can not be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the claimed invention. There must be a teaching or suggestion within the prior art, or within the general knowledge of one skilled in the art, to look to particular sources of information, to select particular elements, and to combine in the way they were combined in the claimed invention. *ATD Corporation v. Lydall, Inc.*, 48 USPQ 2d 1321, 1329 (Fed. Cir. 1998).

It is well established that there must be some motivation or incentive in the cited art to combine the teachings to arrive at the claimed invention as suggested in the Action. *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934, 15 USPQ 2d 1321, 1323 (Fed. Cir. 1990). None of the cited art discloses a delay circuit for delaying initial operation of sensing circuits for a predetermined period each time the supervisory circuit is powered on, or sensing circuits being operable to detect fault conditions, the fault conditions being selected from a group consisting of an open neutral in any one of the AC line inputs, an open first phase, an open second phase, an open third phase, reverse wiring of the first phase to the neutral, reverse wiring of the second phase to the neutral, reverse wiring of the third phase to the neutral, and duplicative wiring of any of the phases. The only suggestion of the claimed combination is in Appellant's disclosure. It is well established that obviousness cannot be established by using Appellant's disclosure to pick and choose between the various elements of the cited art. Identification in the prior art of each individual part of the claimed invention is insufficient to defeat patentability of the claimed invention as a whole. *In re Rouffet*, 47 USPQ2d 1453 (Fed. Cir. 1998).

IX. Conclusion

For the reasons discussed above, the combination of the cited art does not disclose or suggest the claimed system and method for detecting via a three phase supervisory circuit a phase reversal, phase loss, open neutral and undesirable changes in phase voltage levels. In addition, none of the cited art discloses, teaches or suggests delaying sensing circuits or detecting phase differences among three phases. Accordingly, the rejection of claims 1-18 is untenable. Reversal of the final rejection is requested.

Respectfully submitted,



Peter L. Kendall
Reg. No. 46,246

Roylance, Abrams, Berdo & Goodman, L.L.P.
1300 19th Street, N.W., Suite 600
Washington, D.C. 20036
(202) 659-9076

Dated: February 5, 2004

APPENDIX A- COPY OF CLAIMS ON APPEAL

1. A three phase supervisory circuit for detecting fault conditions in an input AC power signal, comprising:

a first sensing circuit for detecting a voltage level for a first phase of said AC power signal and comparing said voltage level of said first phase to a threshold value;

a second sensing circuit for detecting a voltage level for a second phase of said AC power signal and comparing said voltage level of said second phase to said threshold value;

a third sensing circuit for detecting a voltage level for a third phase of said AC power signal and comparing said voltage level of said third phase to said threshold value;

a delay circuit for delaying initial operation of said sensing circuits for a predetermined period each time said supervisory circuit is powered on; and

an activation circuit for receiving indication signals from said sensing and delay circuits, said indication signals indicative of whether said predetermined period of time has elapsed and said voltage levels of said phases have met said threshold value.

2. The three phase supervisory circuit of claim 1, wherein said predetermined time period is approximately between one and two seconds in duration.

3. The three phase supervisory circuit of claim 1, wherein said threshold value is about 12 volts.

4. The three phase supervisory circuit of claim 1, wherein said indication signals represents at least one condition selected from the group consisting of:

a first positive indication that said input AC signal meets the threshold value;

a second positive indication that said predetermined time period elapsed;

a first negative indication that said input AC signal does not meet the threshold value; and

a second negative indication that said predetermined period of time does not elapse.

5. The three phase supervisory circuit of claim 1, wherein said predetermined period of time provides for stabilization of capacitors in said three phase circuit upon initially powering said three phase supervisory circuit.

6. The three phase supervisory circuit of claim 4, wherein in response to receiving said first and second positive indication signals said activation circuit outputs an AC power signal.

7. The three phase supervisory circuit of claim 6, wherein each of said sensing circuits has to detect a proper voltage level in a respective phase before a positive indication is provided to said activation circuit.

8. The three phase supervisory circuit of claim 1, further comprising a contactor coil connected to said activation circuit and a plurality of ground fault circuit interrupter (GFCI) receptacles.

9. The three phase supervisory circuit of claim 8, wherein said GFCI receptacles are protected from AC faults via said three phase supervisory circuit.

10. The three phase supervisory circuit of claim 1, wherein said three phase supervisory circuit operates as a tester for allowing testing of AC power signals.

11. The three phase supervisory circuit of claim 1, wherein said fault conditions comprise at least one of a phase reversal, a phase loss and undesirable changes in a phase voltage level.

12. A method for detecting fault conditions in an input AC power signal via a three phase supervisory circuit, the method comprising:

detecting a voltage level for three phases of said AC input power signal;

comparing said detected phase voltage levels to a threshold value;

delaying initial operation of sensing circuits of said three phase supervisory circuit for a predetermined period each time said supervisory circuit is powered on; and

providing results from said steps of comparing and delaying to an activation circuit.

13. The method of claim 12, wherein said predetermined period is approximately between one and two seconds in duration.

14. The method of claim 13, wherein said predetermined period occurs each time said three phase supervisory circuit is initially powered.

15. The method of claim 12, wherein said threshold value is about 12 volts.

16. The method of claim 12, further comprising:

providing an output AC signal upon a determination that no fault conditions were found in said AC input signal.

17. A three phase supervisory circuit for detecting fault conditions in an input AC power signal, comprising:

a first sensing circuit for detecting a voltage level for a first phase of said AC power signal and comparing said voltage level of said first phase to a threshold value;

a second sensing circuit for detecting a voltage level for a second phase of said AC power signal and comparing said voltage level of said second phase to said threshold value;

a third sensing circuit for detecting a voltage level for a third phase of said AC power signal and comparing said voltage level of said third phase to said threshold value;

a delay circuit for delaying operation of said sensing circuits for a predetermined period of time;

an activation circuit for receiving indication signals from said sensing and delay circuits, said indication signals indicative of whether said predetermined period of time has elapsed and said voltage levels of said phases have met said threshold value; and

at least two of said sensing circuits being operable to detect said fault conditions said fault conditions being selected from a group consisting of an open neutral in any one of the AC line inputs, an open first phase, an open second phase, an open third phase, reverse wiring of the

first phase to the neutral, reverse wiring of the second phase to the neutral, reverse wiring of the third phase to the neutral, and duplicative wiring of any of said phases.

18. A method for detecting ground fault conditions in an input AC power signal via a three phase supervisory circuit, the method comprising:

detecting a voltage level for three phases of said AC input power signal;

comparing said detected phase voltage levels to a threshold value;

delaying operation of said three phase supervisory circuit for a predetermined period;

providing results from said steps of comparing and delaying to an activation circuit; and

determining the existence of said fault conditions from said steps of comparing said detected phase voltage levels, said fault conditions being selected from the group consisting of an open neutral in any one of the AC line inputs, an open first phase, an open second phase, an open third phase, reverse wiring of the first phase to the neutral, reverse wiring of the second phase to the neutral, reverse wiring of the third phase to the neutral, and duplicative wiring of any of said phases.